I. The Drawings Satisfy All Formal Requirements

The Office Action requires drawing corrections in reply to the Office Action. In reply, formal drawings are provided by the Letter to Official Draftsperson attached herewith.

II. The Claims Satisfy the Requirements Under 35 U.S.C. §112, Second Paragraph

The Office Action rejects claims 1-3, 6 and 26-29 under 35 U.S.C. §112, second paragraph, as being indefinite. Specifically, as to claims 1-3, 6 and 26-29, the Office Action objects to the drawings under 37 C.F.R. §1.83(a). This rejection is respectfully traversed.

The Office Action asserts that the following claimed feature is not shown in the drawings: "a light shielding first conductive layer disposed between a semiconductor layer constituting a source region and a drain region of the thin-film transistor and the pixel electrode, the first conductive layer being electrically connected to the semiconductor layer and electrically connected to the pixel electrode." This assertion is respectfully traversed.

As clearly shown in at least Figs. 3, 8, 10 and 14, a light shielding first conductive layer 80a is disposed between a semiconductor layer 1a constituting a source region 1b and a drain region 1c of the thin-film transistor 30 and the pixel electrode 9a, the first conductive layer 80a being electrically connected to the semiconductor layer 1a and electrically connected to the pixel electrode 9a. Thus, the recited feature is clearly shown in the drawings. Withdrawal of the objection to the drawings under 37 C.F.R. §1.83(a) regarding claims 1-3, 6 and 26-29 is respectfully requested.

The Office Action further asserts that it is not clear whether the first and second conductive layers are one same layer or two separate layers. In response, claims 1, 26 and 28 are now amended to clearly recite that a second conductive layer comprises "a film of conductive layer." Withdrawal of the rejection of claims 1-3, 6 and 26-29 under 35 U.S.C. §112, second paragraph is respectfully requested.

III. The Claims Define Patentable Subject Matter

The Office Action rejects claims 1-30 under 35 U.S.C. §102(e) over U.S. Patent 6,067,131 to Sato. This rejection is respectfully traversed.

Sato does not disclose "a thin film transistor disposed in correspondence with intersections of the plurality of data lines and plurality of scanning lines ... a second conductive layer comprising a film of conductive layer, at least partially overlapping the data lines in a plan view," as recited in claim 1, and as similarly recited in claims 26 and 28. Furthermore, claims 26 and 28 further recite that the data line is above the second conductive layer. For example, claim 26 recites "forming the data lines on the second interlayer insulating film above the second conductive layer."

Instead, Sato shows in Figs. 1B, 2B and 3B its semiconductor film 10 disposed along the bus line 9. Furthermore, Fig. 1A also shows a sample light shielding masking pattern 16M disposed above the bus line pattern 9.

For at least these reasons, Sato does not anticipate the subject matter of claims 1-30 under 35 U.S.C. §102(e). Withdrawal of the rejection of claims 1-30 under 35 U.S.C. §102(e) over Sato is respectfully requested.

IV. Conclusion

For at least these reasons, it is respectfully submitted that this application is in condition for allowance. Reconsideration of the application is respectfully requested.

Should the Examiner believe that anything further would be desirable in order to place this application in better condition for allowance, the Examiner is invited to contact Applicant's undersigned representative at the telephone number listed below.

Respectfully submitted,

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Registration No. 27,075

Richard J. Kim
Registration No. 48,360

JAO:RJK/mdw

Attachments:
Appendix
Letter to Official Draftsperson

Date: December 11, 2002

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

APPENDIX

Changes to Claims:

Claim 31 is added.

The following is a marked-up version of the amended claims:

1. (Twice Amended) An electro-optical device, comprising:

a substrate;

a plurality of scanning lines formed above the substrate;

a plurality of data lines formed above the substrate;

a thin-film transistor ~~connected to each of the scanning lines and each of the data lines~~ disposed in correspondence with intersections of the plurality of data lines and the plurality of scanning lines;

a pixel electrode ~~connected to~~ disposed in correspondence with the thin-film transistor;

a light shielding first conductive layer disposed between a semiconductor layer constituting a source region and a drain region of the thin-film transistor, and the pixel electrode, the first conductive layer being electrically connected to the semiconductor layer and electrically connected to the pixel electrode; and

a second conductive layer comprising a film of ~~comprising the first~~ conductive layer, at least partially overlapping the data lines in a plan view.

26. (Twice Amended) A method for fabricating an electro-optical device comprising a substrate, a plurality of scanning lines, a plurality of data lines, a thin-film transistor ~~connected to each of the scanning lines and each of the data lines~~ disposed in correspondence with intersections of the plurality of data lines and the plurality of scanning lines, and a pixel electrode ~~connected to~~ disposed in correspondence with the thin-film transistor, the method comprising the steps of:

forming a semiconductor layer for producing a source region, a channel region, and a drain region on the substrate;

forming an insulating thin film on the semiconductor layer;

forming the scanning lines and one electrode of a storage capacitor on the insulating thin film;

forming a first interlayer insulating film on the scanning lines and the one electrode;

making a first contact hole leading to the semiconductor layer in the insulating film and the first interlayer insulating film;

forming a light-shielding first conductive layer on the first interlayer insulating film so as to be electrically connected to the semiconductor layer through the first contact hole and forming a second conductive layer comprising a film ~~comprising the first~~of conductive layer;

forming a second interlayer insulating film on the first conductive layer and the second conductive layer;

forming the data lines on the second interlayer insulating film above the second conductive layer;

forming a third interlayer insulating film on the data lines;

making a second contact hole leading to the first conductive layer in the second interlayer insulating film and the third interlayer insulating film; and

forming the pixel electrode so as to be electrically connected to the first conductive layer through the second contact hole,

the second conductive layer being formed so as to at least partially overlap the data lines in a plan view.

28. (Twice Amended) A method for fabricating an electro-optical device comprising a substrate, a plurality of scanning lines, a plurality of data lines, a thin-film

transistor ~~connected to each of the scanning lines and each of the data lines~~ disposed in correspondence with intersections of the plurality of data lines and the plurality of scanning lines, and a pixel electrode ~~connected to~~ disposed in correspondence with the thin-film transistor, the method comprising the steps of:

forming a semiconductor layer for producing a source region, a channel region, and a drain region on the substrate;

forming an insulating thin film on the semiconductor layer;

forming the scanning lines and one electrode of a storage capacitor on the insulating thin film;

forming a first interlayer insulating film on the scanning lines and the one electrode of the storage capacitor;

making a first contact hole leading to the semiconductor layer in the first interlayer insulating film;

forming the data lines on the first interlayer insulating film and simultaneously forming an interconnecting conductive layer comprising a film comprising the data lines so as to be electrically connected to the semiconductor layer through the first contact hole;

forming a second interlayer insulating film on the data lines and the interconnecting conductive layer;

making a second contact hole leading to the interconnecting conductive layer in the second interlayer insulating film;

forming a light-shielding first conductive film on the second interlayer insulating film so as to be electrically connected to the interconnecting conductive layer through the second contact hole, and simultaneously forming a second conductive layer comprising ~~the same~~a film ~~as that of the first~~ of conductive layer disposed below the data lines so as to overlap the data lines in a plan view;

forming a third interlayer insulating film on the first conductive layer and the second conductive layer;

making a third contact hole leading to the first conductive layer in the third interlayer insulating film; and

forming the pixel electrode so as to be electrically connected to the first conductive layer through the third contact hole.